IN THE CLAIMS:

1. (Currently Amended) A tracing system, comprising:

a multi-tasking embedded processor, said multi-tasking embedded processor including,

a processor core for executing instructions; and

trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with specified information;

wherein said specified information includes fields to specify an instruction set architecture, an operating mode of said embedded processor, a current process being executed by said multi-tasking embedded processor, and load and store address information, wherein said operating mode is selected from a kernel mode, a supervisor mode, a user mode and a debug mode.

2. (Previously Presented) The tracing system of claim 1, wherein said specified information enables multiple instances of said periodically generated trace synchronization information to be stored at one time in a trace memory.

3. (Previously Presented) The tracing system of claim 2, wherein said multi-tasking embedded processor includes said trace memory.

4. (Previously Presented) The tracing system of claim 2, wherein said multi-tasking embedded processor further includes a trace capture block that receives trace data from said trace generation logic.

5. (Original) The tracing system of claim 4, wherein said trace capture block sends trace data to an off-chip trace memory.

6. (Previously Presented) The tracing system of claim 4, wherein said trace capture block sends trace data to an on-chip trace memory.

7. (Canceled).

8. (Canceled).

9. (Canceled).

10. (Canceled).

11. (Canceled).

12. (Canceled).

13. (Currently Amended) A tracing method, comprising:

periodically generating trace synchronization information in accordance with specified information, said trace synchronization information including program counter information, instruction set architecture information and information that enables a determination of a characteristic of an operating state of a multi-tasking processor, wherein said operating state is selected from a kernel mode, a supervisor mode, a user mode and a debug mode; and

outputting said trace synchronization information to a trace memory.

14. (Canceled).

15. (Canceled).

16. (Previously Presented) The tracing method of claim 13, wherein said characteristic identifies a current process being executed by said multi-tasking processor.

17. (Original) The tracing method of claim 16, wherein said characteristic includes application space identity information.

18. (Original) The tracing method of claim 13, wherein said periodically generated synchronization information includes load and store address information.

19. (Currently Amended) A computer program product comprising:

computer-readable program code for causing a computer to describe an embedded multi-tasking processor, said embedded multi-tasking processor including a processor core for executing instructions, and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with specified information;

wherein said specified information includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an instruction set architecture, an operating mode of said multi-tasking embedded processor, a current process being executed by said multi-tasking embedded processor, and load and store address information, wherein said operating mode is selected from a kernel mode, a supervisor mode, a user mode and a debug mode; and

a computer-usable medium configured to store the computer-readable program codes.

20. (Currently Amended) A computer data signal embodied in a transmission medium comprising:

computer-readable program code for causing a computer to describe a multi-tasking embedded processor, said multi-tasking embedded processor including a processor core for executing instructions, and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with specified information;

wherein said specified information includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an instruction set architecture, an operating mode of said embedded processor, a current process being executed by said multi-tasking embedded processor, and load and store address information, wherein said operating mode is selected from a kernel mode, a supervisor mode, a user mode and a debug mode.

21. (Currently Amended) A method for enabling a computer to generate a tracing system, comprising:

transmitting computer-readable program code to a computer, said computer-readable program code including:

computer-readable program code for causing a computer to describe a multi-tasking embedded processor, said multi-tasking embedded processor including a processor core for executing instructions, and trace generation logic that is operative to periodically generate trace synchronization information, wherein said trace synchronization information is periodically generated in accordance with specified information;

wherein said specified information includes fields to selectively generate software state information within said trace synchronization information, said software state information being selectable from an instruction set architecture, an operating mode of said multi-tasking embedded processor, a current process being executed by said multi-tasking embedded processor, and load and store address information, wherein said operating mode is selected from a kernel mode, a supervisor mode, a user mode and a debug mode.

22. (Original) The method of claim 21, wherein computer-readable program code is transmitted to said computer over the Internet.